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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,774	02/06/2002	Hiroyuki Umeda	93191-000327	7562

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EXAMINER

LAXTON, GARY L

ART UNIT

PAPER NUMBER

2838

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,774	UMEDA, HIROYUKI	
	Examiner Gary L. Laxton	Art Unit 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 18-23 is/are allowed.
- 6) Claim(s) 1-9, 11 and 12 is/are rejected.
- 7) Claim(s) 10 and 13-17 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) Interview Summary (PTO-413) Paper No(s) _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 13-17 are objected to because of the following informalities: claim 13 recites "smaller capability"; this limitation is somewhat vague since it is unclear what is meant by smaller capability. Smaller capability of doing what? Future potential? Conducting current? Resistance? Withstand voltage? Claims 14-17 inherit the same from claim 13. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javanifard et al in view of Yang.

Concerning claims 1 and 2, Javanifard et al discloses a DC/DC converter (figure 1), two charge pump circuits (110, 120) each of which converts DC into a given DC output voltage; and two driving circuits driving the two charge pumps (for example see figure 2: VCO 240 and 241); wherein in a first mode (switch 130 is “on” and switch 131 is “on”) the given output voltage is output from each of the two charge pump circuits (node 150 of figure 1), and wherein in a second mode (switch 130 is “off” and switch 131 is “off”), one of the two driving circuits drives one of the two charge pump circuits, and the given output voltage is output from one of the two charge pump circuits and is not output from the other one of the two charge pump circuits (col. 3 lines 25-35: when switch 130 and 131 are “off” one charge pump is “on” and the other is “off”).

However, Javanifard et al do not disclose the two driving circuits complementarily driving the two charge pump circuits. Nor does Javanifard et al disclose stopping an operation thereof of the other one of the two charge pump circuits in the second mode.

Yang teaches using at least two charge pumps to produce a pumped voltage (VPPI) by driving the two charge pumps (71, 72) with non-overlapping clock signals (OSC and OSC inverter: as indicated by the inverter (60)).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use two driving circuits that complementarily drive the two charge pump circuits as taught by Yang in order to drive one pump at a time in order to avoid producing high currents by driving both pumps at once. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use to stop an operation thereof of

the other one of the two charge pump circuits in the second mode in order to reduce the output voltage by the amount of that specific charge pump output.

Concerning claim 3, a control input terminal (control input for switches 130/131) in which a signal indicating the second mode is input.

Concerning claims 4 and 6, the first mode is set when a load connected to each of the two charge pump circuits is large, and the second mode is set when the load is small (col. 5 lines 65-67; col. 6 lines 34-60; col. 8 lines 24-45: first mode when the output voltage is high and second mode when the voltage is low to conserve power or in read write operations).

Concerning claim 5, Javanifard et al discloses the claimed invention as stated above in regards to claim 1 except for the first mode is set when the DC input voltage is low, and the second mode is set when the DC input voltage is high.

Javanifard et al do teach controlling the switches, (130 and 131), and therefore controlling whether both pumps are on or if only one is on, as a function of such parameters as the available power supply (col. 5 lines 65-67; col. 7 lines 1-5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use set the first mode when the DC input voltage is low, and the second mode is set when the DC input voltage is high in order to engage both pumps when the input is low in order to boost the input much higher to satisfy the regulated output demand and to use only one pump when the input is high in order to avoid boosting the output voltage too high and overload the output load.

6. Claims 7-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banba et al in view of the admitted prior art figures 6 and 8.

Concerning claim 7, Banba et al disclose a DC/DC converter (figure 5) having a charge pump circuit (22); oscillation circuit (21) which supplies an oscillation output; and wherein the oscillation circuit (21) varies a frequency of the oscillation output ("on" or "off") according to an operation mode (e.g. mode 1 when the output is lower than 10v and mode two when the output is greater than 10v).

However, Banba et al does not show a driver circuit which drives the charge pump.

The admitted prior art figures 6 and 8 both illustrate driver circuits connected between the oscillator and charge pump for receiving the clock signal and driving the charge pump.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use driver circuits to drive the charge pump in order to buffer the clock signals from the oscillator.

Concerning claims 8 and 12, in mode 1 the voltage is below 10v and the oscillator outputs a clock signal at a specified frequency; when in mode 2 the voltage is greater than 10v and the oscillator is shut off resulting in a zero hertz frequency.

Concerning claim 9, input terminal (CPE) inputs a signal (CPE) indicating the second mode is input (col. 7 lines 49-51: CPE is low = oscillator "off").

7. Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka in view of the admitted prior art figures 6 and 8.

Concerning claim 7, Fujioka discloses a DC/DC converter (figure 1) having a charge pump circuit (20); oscillation circuit (10 and 30) which supplies an oscillation output (40); and wherein the oscillation circuit (10 and 30) varies a frequency of the oscillation output (40, 41, 42; F_s – high frequency and f_o – low frequency) according to an operation mode (considered start/stop or start/conserve: abstract).

However, Fujioka does not show the driver circuit which drives the charge pump.

The admitted prior art figures 6 and 8 both illustrate driver circuits connected between the oscillator and charge pump for receiving the clock signal and driving the charge pump.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use driver circuits to drive the charge pump in order to buffer the clock signals from the oscillator.

Concerning claim 8, F_s is the higher frequency and f_o is lower frequency. The higher frequency is set during the start mode and the lower frequency is set during the second conserve mode.

Concerning claim 9, the control input from selection circuit (50) sends a signal indicating the second mode is input.

Concerning claim 11, the first mode is set when Vcc (input voltage) is low and the second mode is set when Vcc is high (e.g. after power up).

Allowable Subject Matter

8. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 13-17 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

10. Claim 18-23 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter:

Concerning claim 10, prior art fails to disclose or suggest, *inter alia*, a dc/dc converter comprising a first mode is set when a load connected to the charge pump is large and a second mode is set when the load is small.

Concerning claims 13-17, prior art fails to disclose or suggest, *inter alia*, a dc/dc converter comprising a driving circuit that uses a first switching circuit to drive a charge pump circuit in a first mode and uses a second switching circuit to drive a charge pump circuit in a second mode.

Concerning claims 18-23, prior art fails to disclose or suggest, *inter alia*, a power supply apparatus comprising a selection circuit which selects an oscillation output; and a timing signal generation circuit which generates a given timing signal to be supplied to each of the first stage

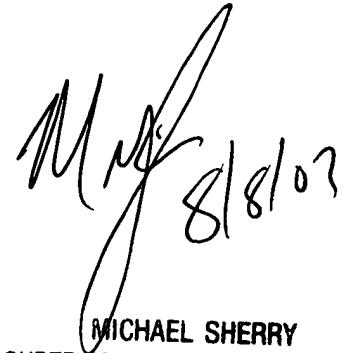
Art Unit: 2838

driving circuit and a second stage driving circuit based on a signal that is selected by the selection circuit..

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (703) 305-7039. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (703)308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-9306 for regular communications and (703)-872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
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GLL
August 6, 2003